Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] A method of preventing exposure of at least one layer of a semiconductor device, the method comprising the steps of:
etching an opening through an interlevel dielectric (ILD) layer and leaving a remaining portion of an underlying cap layer;
maintaining the semiconductor device in an inert gas; and
forming a portion of a liner in the opening to prevent exposure of the ILD layer during subsequent processing.

[c2] The method of claim 1, wherein the remaining portion is no less than approximately 10% of the underlying cap layer thickness and no greater than approximately 90% of the underlying cap layer thickness.

[c3] The method of claim 1, wherein the portion of the liner is no less than approximately 5% of a total liner thickness and no greater than approximately 30% of the total liner thickness.

[c4] The method of claim 3, wherein the portion of the liner is no less than approximately 10% of the total liner

thickness and no greater than approximately 20% of the total liner thickness.

[c5] The method of claim 1, wherein the subsequent processing includes:
etching through the portion of the liner and the portion of the underlying cap layer to expose a metal layer; and
forming a via in the opening.

[c6] The method of claim 1, further comprising the step of degassing prior to the liner forming step.

[c7] The method of claim 1, wherein the inert gas is selected from the group consisting of:
argon and nitrogen.

[c8] A method of forming a via in a semiconductor device, the method comprising the steps of:
first etching an opening through an interlevel dielectric (ILD) layer and leaving a remaining portion of an underlying cap layer;
maintaining the semiconductor device in an inert gas;
forming at least a portion of a liner in the opening to prevent exposure of the ILD layer;
second etching through the at least a portion of the liner and the portion of the underlying cap layer to expose a metal layer; and

forming the via in the opening.

[c9] The method of claim 8, further comprising the step of degassing prior to the liner forming step.

[c10] The method of claim 8, wherein the second etching step is conducted in an etching chamber.

[c11] The method of claim 8, wherein the second etching is conducted in a liner deposition chamber.

[c12] The method of claim 8, wherein the remaining portion is no less than approximately 10% of the underlying cap layer thickness and no greater than approximately 90% of the underlying cap layer thickness.

[c13] The method of claim 8, wherein the portion of the liner is no less than approximately 5% of a total liner thickness and no greater than approximately 30% of the total liner thickness.

[c14] The method of claim 14, wherein the portion of the liner is no less than approximately 10% of the total liner thickness and no greater than approximately 20% of the total liner thickness.

[c15] The method of claim 8, wherein the portion of the liner includes tantalum nitride.

[c16] A method of forming a via in a semiconductor device, the method comprising the steps of:
first etching an opening through an organic interlevel dielectric (ILD) layer and leaving a remaining portion of an underlying cap layer to maintain a metal layer thereunder sealed;
maintaining the semiconductor device in an inert gas;
degassing the semiconductor device;
forming at least a portion of a liner in the opening to prevent exposure of the ILD layer in a chamber;
second etching through the portion of the liner and the portion of the underlying cap layer to expose the metal layer in the chamber; and
forming the via in the opening.

[c17] The method of claim 16, wherein the remaining portion is no less than approximately 10% of the underlying cap layer thickness and no greater than approximately 90% of the underlying cap layer thickness.

[c18] The method of claim 16, wherein the portion of the liner is no less than approximately 5% of a total liner thickness and no greater than approximately 30% of the total liner thickness.

[c19] The method of claim 18, wherein the portion of the liner is no less than approximately 10% of the total liner

thickness and no greater than approximately 20% of the total liner thickness.

[c20] The method of claim 16, wherein the portion of the liner includes tantalum nitride.